

What is claimed is:

1 1. A method for forming a volatile memory structure,
2 comprising the steps of:
3 providing a substrate having a pair of neighboring
4 trenches;
5 forming a buried trench capacitor in a lower portion of
6 each trench;
7 forming an asymmetric collar insulating layer, having a
8 high level portion and a low level portion, over
9 an upper portion of the sidewall of each trench,
10 and forming a conductor layer, overlying the
11 buried trench capacitor in each trench, below the
12 surface of the substrate with a lower part of the
13 conductive layer surrounded by the asymmetric
14 collar insulating layer, wherein the high level
15 portion of the asymmetric collar insulating layer
16 is adjacent to the substrate between the
17 neighboring trenches and the low level portion is
18 covered by an upper part of the conductive layer;
19 forming a dielectric layer overlying the conductive
20 layer in each trench; and
21 forming two access transistors on the substrate outside
22 of the pair of the neighboring trenches,
23 respectively, wherein the two access transistors
24 have source/drain regions electrically connecting
25 to the conductive layer.

1 2. The method as claimed in claim 1, wherein the step
2 of forming the asymmetric collar insulating layer and the
3 conductive layer, comprises:

4 forming a first conductive layer overlying the buried
5 trench capacitor in each trench and surrounded by
6 an insulating spacer protruding the surface of
7 the first conductive layer;

8 covering portions of the insulating spacers adjacent to
9 the substrate between the neighboring trenches by
10 a masking layer;

11 removing the uncovered insulating spacers to form the
12 asymmetric collar insulating layer in each
13 trench;

14 removing the masking layer; and

15 forming a second conductive layer overlying the first
16 conductive layer, wherein the first conductive
17 layer and the second conductive layer are
18 combined as the conductive layer.

1 3. The method as claimed in claim 2, wherein the
2 masking layer is a photoresist layer.

1 4. The method as claimed in claim 1, wherein the step
2 of forming the asymmetric collar insulating layer,
3 comprises:

4 forming a sacrificial layer overlying the buried trench
5 capacitor in each trench and surrounded by an
6 insulating spacer protruding the surface of the
7 sacrificial layer;

8 covering portions of the insulating spacers adjacent to
9 the substrate between the neighboring trenches by
10 a masking layer;
11 removing the uncovered insulating spacers to form the
12 asymmetric collar insulating layer; and
13 successively removing the masking layer and the
14 sacrificial layer.

1 5. The method as claimed in claim 4, wherein the
2 sacrificial layer is a photoresist or anti-reflection layer.

1 6. The method as claimed in claim 4, wherein the
2 masking layer is a photoresist layer.

1 7. The method as claimed in claim 1, wherein the
2 conductive layer is a doped polysilicon layer.

1 8. The method as claimed in claim 1, wherein before
2 the step of forming the dielectric layer, further comprises:
3 forming active area/isolation areas through an active
4 area masking layer.

1 9. The method as claimed in claim 8, wherein the
2 active area masking layer is a strap type pattern.

1 10. The method as claimed in claim 1, further forming
2 a gate on the dielectric layer over each trench.

1 11. A volatile memory structure, comprising:
2 a substrate having a pair of neighboring trenches;
3 two buried trench capacitors respectively disposed in a
4 lower portion of the neighboring trenches;

5 two conductive layers respectively disposed overlying
6 the buried trench capacitor in each trench and
7 below the surface of the substrate;
8 two asymmetric collar insulating layers respectively
9 disposed over an upper portion of the sidewall of
10 the neighboring trenches and surrounding a lower
11 part of the conductive layers, wherein the
12 asymmetric collar insulating layer has a high
13 level portion and a low level portion, each high
14 level portion is adjacent to the substrate
15 between the neighboring trenches, and each low
16 level portion is covered by an upper part of the
17 conductive layer;
18 two dielectric layers respectively disposed overlying
19 the conductive layer in each trench; and
20 two access transistors respectively disposed overlying
21 the substrate outside of the pair of the
22 neighboring trenches and having source/drain
23 regions electrically connecting to the conductive
24 layers, respectively.

1 12. The volatile memory structure as claimed in claim
2 11, further comprising two gates respectively disposed
3 overlying the dielectric layer over each trench.

1 13. The volatile memory structure as claimed in claim
2 11, wherein the conductive layer is a doped polysilicon
3 layer.

1 14. A method for forming a trench capacitor structure
2 for a volatile memory device, comprising the steps of:

3 providing a substrate having a trench;
4 forming a buried bottom plate in the substrate around a
5 lower portion of the trench;
6 forming a capacitor dielectric layer over a lower
7 portion of the sidewall of the trench ;
8 forming a top plate in the trench and surrounded by the
9 capacitor dielectric layer;
10 forming an asymmetric collar oxide layer, having a high
11 level portion and a low level portion, over an
12 upper portion of the sidewall of the trench, and
13 forming a conductive layer, overlying the top
14 plate in the trench, below the surface of the
15 substrate with a lower part of the conductive
16 layer surrounded by the asymmetric collar oxide
17 layer, wherein the low level portion of the
18 asymmetric collar oxide layer is covered by an
19 upper part of the conductive layer; and
20 forming a dielectric layer overlying the conductive
21 layer in the trench.

1 15. The method as claimed in claim 14, wherein the
2 step of forming the asymmetric collar oxide layer and the
3 conductive layer, comprises:

4 forming a first conductive layer overlying the top
5 plate in the trench and surrounded by an oxide
6 spacer protruding the surface of the first
7 conductive layer;
8 covering a portion of the oxide spacer by a masking
9 layer;

10 removing the uncovered oxide spacer to form the
11 asymmetric collar oxide layer in the trench;
12 removing the masking layer; and
13 forming a second conductive layer overlying the first
14 conductive layer, wherein the first conductive
15 layer and the second conductive layer are
16 combined as the conductive layer.

1 16. The method as claimed in claim 15, wherein the
2 masking layer is a photoresist layer.

1 17. The method as claimed in claim 14, wherein the
2 step of forming the asymmetric collar oxide layer,
3 comprises:

4 forming a sacrificial layer overlying the top plate in
5 the trench and surrounded by an oxide spacer
6 protruding the surface of the first masking
7 layer;
8 covering a portion of the oxide spacer by a masking
9 layer;
10 removing the uncovered oxide spacer to form the
11 asymmetric collar oxide layer; and
12 successively removing the masking layer and the
13 sacrificial layer.

1 18. The method as claimed in claim 17, wherein the
2 sacrificial layer is a photoresist or anti-reflection layer.

1 19. The method as claimed in claim 17, wherein the
2 masking layer is a photoresist layer.

1 20. The method as claimed in claim 14, wherein the
2 conductive layer is a doped polysilicon layer.

1 21. The method as claimed in claim 14, wherein before
2 the step of forming the dielectric layer, further comprises:
3 forming active area/isolation areas through an active
4 area masking layer.

1 22. The method as claimed in claim 21, wherein the
2 active area masking layer is a strap type pattern.

1 23. A trench capacitor structure for a volatile memory
2 device, comprising:
3 a substrate having a trench;
4 a buried bottom plate formed in the substrate around a
5 lower portion of the trench;
6 a capacitor dielectric layer disposed in the lower
7 portion of the trench;
8 a top plate disposed in the trench and surrounded by
9 the capacitor dielectric layer;
10 a conductive layer disposed overlying the top plate in
11 the trench and below the surface of the
12 substrate;
13 an asymmetric collar oxide layer disposed over an upper
14 portion of the sidewall of the trench and
15 surrounding a lower part of the conductive layer,
16 wherein the asymmetric collar oxide layer has a
17 low level portion covered by an upper part of the
18 conductive layer; and

Client's ref.: 92040US
Our ref: 0593-10195US, final, 王琮邨(spin)

19 a dielectric layer disposed overlying the conductive
20 layer in the trench.

1 24. The trench capacitor structure as claimed in claim
2 23, wherein the conductive layer is a doped polysilicon
3 layer.